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A Maskless Laser-Write Lithography Processing of Thin-Film Transistors

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Abstract
We report on a fabrication method of the hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) using a maskless laser-write lithography (LWL). Level-to-level alignment with a high accuracy is demonstrated using LWL method. The obtained results show that it is possible to fabricate a-Si:H TFTs using a well-established a-Si:H TFT technology in combination with the maskless lithography. This approach can be extended to very large scale areas.

1. Introduction
Optical maskless lithography technology has drawn increasing attentions in recent years for its advantages such as: fast turn-around time and no cost for mask-making, flexibility in lithographic process and capability for large area exposure [1-3]. When a low-volume and a fast run is necessary, mask-based lithographic process is not a best option. In flat panel display and solar-cell panel processing, as substrate sizes increase, the cost of mask fabrication rapidly increases with the size. To reduce the fabrication cost of the masks, a laser direct patterning technology of thin-film has been investigated [3, 4]. It is recently reported that laser direct patterning of ITO thin-film can compete with the typical photolithography [5]. At the same time, there have been increasing efforts to develop optical maskless lithography technology for the semiconductor industry. As chip designs become more complex with smaller critical dimension, the cost and time of mask-making increase [6].

In this work, we used a maskless laser-write lithography (LWL) system of Heidelberg Instruments (DWL 4000) which has been a workhorse for a mask-making process in large area applications. We describe the feasibility of the using LWL system together with level-to-level alignment in fabrication of the a-Si:H TFTs. Also electrical performances of the fabricated a-Si:H TFTs on flat surface are described.

2. Fabrication method and results
The LWL system (DWL 4000) is capable of creating 2D and complex 3D structures on up to 400 mm x 400 mm substrate using binary and gray-scale exposure, respectively. Figure 1 shows the optical design and write strategy of the system; the acousto-optic modulator (AOM) modulates the laser beam intensity, and the acousto-optic deflector (AOD) deflects the laser beam and performs a scan [7]. After scanning the entire area of the moving substrate with a programmed scan width, stitching of those stripes is performed. Modified optical set-ups provide various write-modes with different writing speed and resolution (Table 1) [7]. The performance specifications of the adopted write-mode (II) for the present study are as follows: the minimum feature size of 0.7 µm can be achieved with an address grid of 20 nm. The focal length of the write lens is 4 mm and the writing speed is 101 mm^2/min. The alignment accuracy is 0.25 µm.

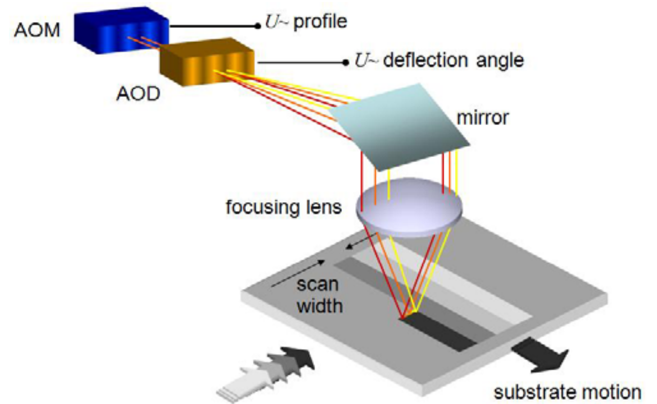

Figure 1 The optical design and writing strategy. The substrate moves in the x-y plane during the exposure.

The LWL system was used to expose all device layers before each etching processing step. The photoresist (S1805) is spin-coated at 2000 rpm and soft-baking is performed over a hotplate at 100 °C for 1 min. Then LWL exposure is conducted, which is followed by a development process in AZ 726 and a hard-baking over a hotplate at 110 °C for 5 min.

Write Mode	I	II	III	IV
Address Grid [nm]	10	20	25	50
Minimum Feature Size [µm]	0.6	0.7	0.8	1.6
Write Speed [mm^2/min]	26	101	155	560
Edge Roughness [3σ, nm]	60	80	100	120

Table 1 Specifications of the LWL system for different write mode.

First, Cr of 200 nm was deposited by a sputtering method and then the Cr gate electrode was patterned by wet-etching using CR-14 etchant (layer #1). Next, PECVD was used to deposit a tri-

layer of gate silicon nitride (a-SiN_X:H, 400 nm) forming a gate insulator together with amorphous silicon (a-Si:H, 170 nm) and phosphorous-doped (n+) a-Si:H (70 nm) forming an active channel layer. The active island was defined by RIE dry-etching of the a-Si:H and n+a-Si:H using a gas mixture of SF_6 and O_2 (layer #2). Following a deposition of a source/drain (S/D) metal Cr layer (130 nm) by a sputtering method, wet-etching using CR-14 etchant was done to form S/D contacts (layer #3). Then to remove the n+ a-Si:H layer from the channel region, back-channel etching is performed by RIE dry-etching with a gas mixture of SF_6 and O_2 using the S/D metal and a photoresist as a mask. We subsequently defined contact via to the gate electrode using buffered hydrofluoric acid (BHF) (layer #4). As a final step, thermal annealing was performed at 250 °C for an hour to improve electrical properties of each film layer. Fig.2 (a) shows an example of the fabricated a-Si:H TFT.

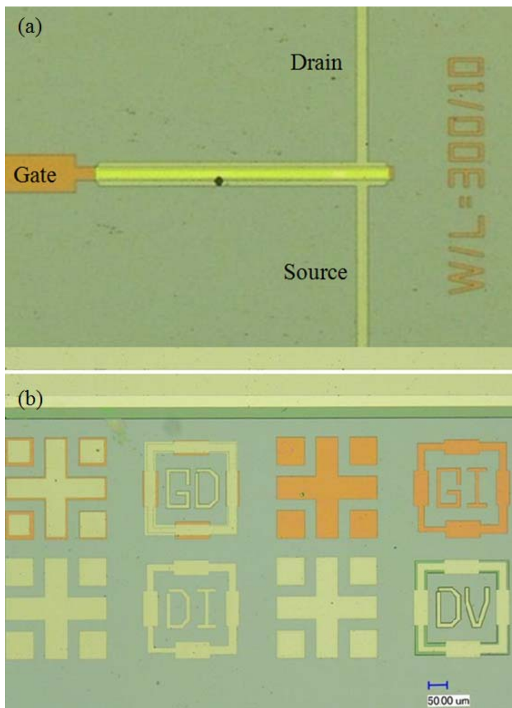

Figure 2 An optical microscope images: (a) the fabricated a-Si:H TFT (b) the alignment marks.

Level-to-level alignment with a high accuracy is the central critical issue for fabricating fully functional devices and circuits. It was performed here in the following manner: the optical and metrology system in the LWL is equipped with two camera systems. One camera with a large field of view is used to locate alignment marks and another camera with high resolution is intended for aligning these marks. Fig. 2 (b) shows part of the alignment marks used in this experiment. The level-to-level alignment error is defined as the relative position deviation of the alignment marks within the two following layers, and we derive vertical and horizontal deviation from the measurement of the distance of the borders on four sides in the bar alignment mark. The measured error was less than 2.5 µm for TFT with a 10 µm channel length and up to 300 µm channel width. To evaluate LWL exposure accuracies, we measured dimensions of various structures. The discrepancy between fabricated structures and an electronic design was about 7 %.

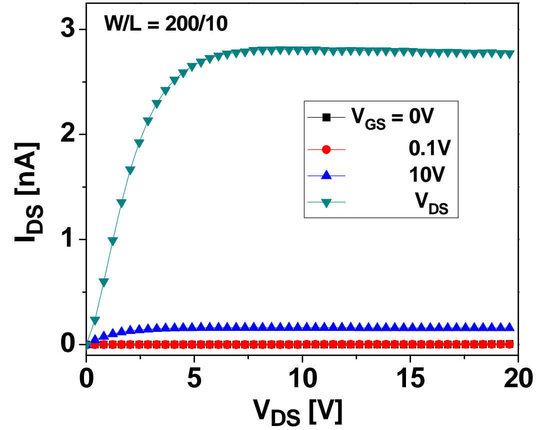

Figure 3 Output characteristics of the fabricated a-Si:H TFT.

Electrical measurements were conducted and analyzed using a probe station in combination with HP 4156 at room temperature in a dark condition. We first measured the output characteristics of the TFT for various gate voltages (V_{GS}) (Fig. 3). Then the transfer characteristics for drain-to-source voltage (V_{DS}) of 0.1 V and V_{GS} were measured (Fig. 4). We extracted the field-effect mobility (μ_{FE}) and threshold voltage (V_{th}) by using the maximum slope method [8]. The subthreshold swing (*SS*) is defined as the steepest slope of the I_{DS}-V_{GS} plot in log scale. Table 2 shows the summary of the extracted TFT parameters that can be improved through a process optimization. We successfully demonstrated a-Si:H TFTs with reasonable electrical performance (μ_{FE} ~ 0.25 cm^2 /V·s, and V_{th} ~ 4.9V) on a hemispherical glass substrate [9]. An extensively modified LWL system with more optimized TFT process conditions was used; the modified LWL system is capable of tilting the substrate to make incident write-beam perpendicular to the local exposed surface.

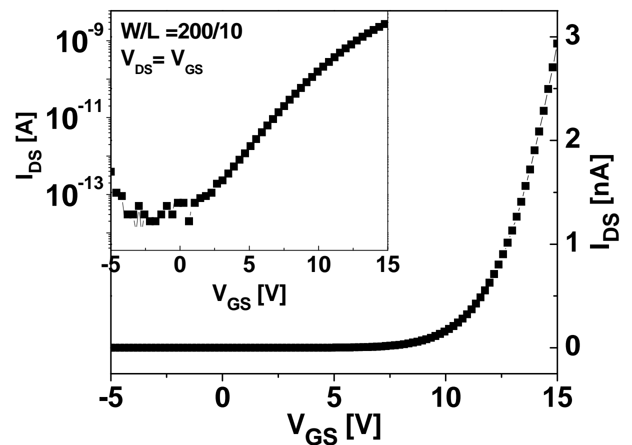

Figure 4 Transfer characteristics of the fabricated a-Si:H TFT in saturation operation regime. Inset shows it in a log scale.

Parameters	V_{DS} = 0.1 V	$V_{DS} = V_{GS}$
V_{th} [V]	9.29	10.2
μ_{FE} [cm^2 /V·s]	3.4x10^{-4}	7.2x10^{-4}
On/Off Current Ratio	5.2x10^3	2.9x10^5
SS [V/dec]	2.7	2.3

Table 2 Summary of the extracted TFT (W/L = 200/10) parameters.

3. Conclusion

In summary, the a-Si:H TFTs with a 10 µm channel length were fabricated using the maskless laser-write lithography in combination with the well-established a-Si:H TFT processing technology. It is very easy to modify the device and circuit designs during process development since lithographic processing is performed directly from an electronic design rather than from the photolithographic mask. This fabrication method using LWL can be an alternative to conventional photolithography for rapid and low-volume prototyping by reducing turn-around time and cost of mask fabrication process. This proposed fabrication technique can be extended from research to development and fabrication of large area electronics including flat panel displays, X-ray image sensors, and solar panel processing.

4. Acknowledgements

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